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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,665	12/21/2001	Kazuhiko Yoshizawa	16869P-035900US	5071

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EXAMINER	
YENKE, BRIAN P	

ART UNIT	PAPER NUMBER
2614	

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,665	YOSHIZAWA ET AL.	
	Examiner	Art Unit	
	BRIAN P. YENKE	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Response (08 Oct 04)*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's arguments filed 08 October 2004 have been fully considered but they are not persuasive.

Applicant's Arguments

a) Applicant states that JP 60-185482 utilizes a grid pattern having non-uniformly spaced grid lines, which are spaced apart differently (i.e. more closely) at the perimeter of the display than in the central region of the display, however the computed correction values are then delivered to a D/A converter at a constant period to produce a correction signal.

Examiner's Response

a) Initially the examiner would like to point out that neither claims 7 or 9 include any language/limitation regarding the feeding of correction points at a varying rate for producing a correction signal. Also, the examiner upon review of JP 60-185482 (Applicant's cited prior art), acknowledges that PLL circuit 1 forms a fCLK 1 being a frequency N-times fH and a frequency fCLK2 being a frequency M times from a clock signal obtained through MxN multiple of the horizontal deflection frequency, where a counter 17 counts the fCLK2 of the longitudinal line. Thus if the correction points/grid lines of the pattern are spaced apart differently, than the points are corrected at different times, since points that are closer together have a shorter period of time to be corrected, than points that are more spread out. If the applicant disagrees with this point, the examiner requests the applicant to explain/clarify how points that are spaced apart

differently are corrected in an constant period, when points that are closer together are corrected in a shorter time interval than more widely spaced points.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 7 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by JP-60-185482.

In considering claims 7 and 9,

As disclosed by applicant, JP-60-185482 (see applicant's specification pages 1-2) the applicant discloses that prior art utilizes a convergence correction method where the interval between the vertical lines in the perimeter of the screen (both right and left edges) becomes closer than that in a central portion of the screen (see JP-60-185482 Figures 1-4). Regarding the claimed analog signal generator, memory, and address generation circuit see AAPA pp 1-2 and JP-60-185482 (Fig 1).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3a. Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heizman et al., US 6,108,054 in view of JP-60-185482.

In considering claims 1-3, 7, 9, 16-17, 22-24 and 27,

a) the claimed a color display apparatus is met screen 280 (Fig 2).

b) the claimed circuitry having an input to receive a television signal...is met by video section 225 (Fig 2) which receives the demodulated/tuned TV signal via antenna 200, tuner 205 and demodulator 210 (Fig 2).

c) the claimed a convergence correction signal...is met by uC 235, non-volatile memory 240, volatile memory 245 and DAC 250, which receives the horizontal and vertical sync signals from signal processing unit 230.

c-1) the claimed a memory...is met by non-volatile memory 240 which stores the correction interpolated point values and memory 240 which stores the computed results based upon the horizontal and vertical sync signals received from signal processing unit 230.

c-2) the claimed a address generation circuit...is met by uC 235 which selects the appropriate the values and carries out the appropriate interpolation method.

c-3) the claimed an analog signal generation circuit...is met by DAC array 250 (Fig 2).

However, Heizmann does not explicitly recite generating an address at a variable rate.

Heizmann does disclose a system which obtains correction values for convergence by calculating the values for the video lines of a first field of the video frame, which is used to correct neighboring lines in different video fields, thus saving memory/computation.

The examiner incorporates JP-60-185482, which discloses a system that utilizes a convergence correction method where the interval between the vertical lines in the perimeter of the screen (both right and left edges) becomes closer than that in a central portion of the screen, making the convergence correction of the edges easier (AAPA page 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Heizmann which is concerned with convergence correction of a display, by utilizing a convergence method where the interval between the vertical lines in the perimeter of the screen are closer than those in the central portion of the screen, which would easier correct the edges, which would subsequently generate addresses at different rates, since the points on the edges are closer, they would require computation/calculation at a fast rate than points which are spread apart further (central portion).

In considering claims 5-6, 8, 13-14, 18-20 and 25,

Neither Heizmann, nor JP-60-185842 disclose (from the translated abstract) the LPF and filter parameter selection circuit, these are notoriously well known elements in a convergence correction system, where the amount of filtering performed is based upon the filter's characteristics and the received signal.

Thus the examiner takes OFFICIAL NOTICE, regarding a LPF which alters a filter parameter value.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify JP-60-185482 which performs convergence correction, where based upon the area of the display determines the amount of correction, by utilizing a conventional LPF and selection circuit in order to provide a correction signal which has been selectively filtered based upon the amount of correction required for display.

In considering claim 21,

a) the claimed D/A is met by DAC array 250

b) the claimed convergence yoke is met by vertical and horizontal deflection coils, 261/266/271 and 262/267/272 respectively.

Neither Heizman nor JP-60-185482 (from translated abstract) discloses the use of an amplifier 255 however, Heizman does not explicitly recite the type of amplification.

Although the use of a LPF in conjunction with another amplifier is notoriously well known, the examiner takes "OFFICIAL NOTICE", since the use of a LPF to remove high frequencies, where a coupled amplifier is used to

amplify the clean (high frequencies removed) signal in order to provide a device an ideal signal.

Therefore, it would have been obvious to one of ordinary skill in the are at the time of the invention to modify Heizmann which is concerned with convergence correction of a display, and JP-60-185482 which discloses convergence method where the interval between the vertical lines in the perimeter of the screen are closer than those in the central portion of the screen, which would easier correct the edges, by implementing conventional LPF coupled with amplifiers in order to provide the device (CRT's in this instance) a amplified signal which is noise free (free of high frequencies).

In considering claims 10-12, 15 and 26,

Neither Heizman nor JP-60-185482 does not explicitly disclose (from the translated abstract) the separation of the memory location spacing based upon the 1st and 2nd pair of adjacent convergence correction data.

Heizmann does disclose a system which obtains correction values for convergence by calculating the values for the video lines of a first field of the video frame, which is used to correct neighboring lines in different video fields, thus saving memory/computation.

However, JP-60-185482 does disclose, as admitted by applicant's own disclosure (see own disclosure, pp 1-2) that the correction method utilized by JP-60-185482, based upon the area of correction uses a closer interval between the vertical lines in the perimeter of the screen (both right and left edges) than that in a central portion of the screen.

Therefore, since the spacing between the 1st (edges) and 2nd pair (central portion) convergence correction data are different, one of ordinary skill in the art at the time of the invention would modify Heizmann and JP-60-185482 by utilizing an addressing scheme/memory locations which are also different, by simply spacing the edges and the central portion in different memory locations.

3b. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP-60-185482.

In considering claim 8,

Although, JP-60-185842 does not explicitly disclose (from the translated abstract) the LPF and filter parameter selection circuit, these are notoriously well known elements in a convergence correction system, where the amount of filtering performed is based upon the filter's characteristics and the received signal.

Thus the examiner takes OFFICIAL NOTICE, regarding a LPF which alters a filter parameter value.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify JP-60-185482 which performs convergence correction, where based upon the area of the display determines the amount of correction, by utilizing a conventional LPF and selection circuit in order to provide a correction signal which has been selectively filtered based upon the amount of correction required for display.

In considering claim 9,

Although, JP-60-185482 does not explicitly disclose (from the translated abstract) the separation of the memory location spacing based upon the 1st and 2nd pair of adjacent convergence correction data.

However, JP-60-185482 does disclose, as admitted by applicant's own disclosure (see own disclosure, pp 1-2) that the correction method utilized by JP-60-185482, based upon the area of correction uses a closer interval between the vertical lines in the perimeter of the screen (both right and left edges) than that in a central portion of the screen.

Therefore, since the spacing between the 1st (edges) and 2nd pair (central portion) convergence correction data are different, one of ordinary skill in the art at the time of the invention can utilize an addressing scheme/memory locations which are also different, by simply spacing the edges and the central portion in different memory locations.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will

the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Yenke whose telephone number is (703) 305-9871. The examiner work schedule is Monday-Thursday, 0730-1830 hrs.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, John W. Miller, can be reached at (703)305-4795.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is

(703)305-HELP.

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PAIR (http://pair.uspto.gov) provides customers direct secure access to their own patent application status information, as well as to general patent information publicly available. EFS allows customers to electronically file patent application documents securely via the Internet. EFS is a system for submitting new utility patent applications and pre-grant publication submissions in electronic publication-ready form. EFS includes software to help customers prepare submissions in extensible Markup Language (XML) format and to assemble the various parts of the application as an electronic submission package. EFS also allows the submission of Computer Readable Format (CRF) sequence listings for pending biotechnology patent applications, which were filed in paper form.

BRIAN P. YENKE
Primary Examiner
Art Unit 2614

B.P.Y
25 February 2005